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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,288	02/09/2004	Soo-doo Chae	249/380	8741

7590 07/21/2005

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,288	CHAE ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-28 and 44-55* is/are pending in the application.

4a) Of the above claim(s) *22-28 and 49-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-16,19-21 and 44-48* is/are rejected.

7)☒ Claim(s) *17,18 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 44-48, 1-21, and 55 in the reply filed on 06/02/05 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12, 14-16, 19-21, and 44-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAAP) of this application in combination with Mort et al. (US patent 4,544,617).

With respect to claim 44, AAPA teaches a single electron transistor having memory function comprising (see figs. 1-2 and associated of the specification of this application):

a substrate 30 including a source region 34a, a channel region 34b, and a drain region 34c;

a trap layer 36a,36b (since they are made of silicon nitride and located in the location as claimed) formed on the substrate; and

a gate electrode 40 opposite the trap layer, wherein the trap layer has an interval therein such that at least one quantum dot 34d can be formed in same interval in the channel region.

With respect to claim 46, AAPA further teaches that the size of quantum dot is less 0.1 nm.

With respect to claim 47, AAPA further teaches the trap layer is made of nitride.

With respect to claim 6, AAPA further teaches the trap layer includes at least two trap sections separated by the interval.

With respect to claims 5, 7, 16, and 21, AAPA further teaches the at least two trap sections are a nitride layer.

With respect to claim 8, AAPA further teaches an insulation film (upper part of 42) covering the at least two trap sections.

With respect to claim 10, AAPA fails to teach that the interlayer insulator is made of oxide.

However, the use of oxide as interlayer insulator material is well-known.

With respect to claims 4, 11 and 15, AAPA further teaches a size of the at least one quantum dot is 0.1 nm or less.

With respect to claim 12, AAPA further teaches the gate electrode includes conductive spacers separated by the interval.

With respect to claim 14, AAPA teaches the conductive spacers are made of polysilicon but fails to teach the conductive spacers are made of silicon.

However, the use of silicon as conductive spacer material is well-known.

With respect to claim 19, AAPA further teaches an insulation film (part of 42 between 38a,38b) on and between the at least two trap sections.

With respect to claims 1 and 45 , AAPA further teaches an insulator (bottom part of 42) formed between the substrate and the trap sections but fails to teach that the insulation film function as tunneling layer.

However, AAPA teaches the claimed structure, the insulator would inherently act as tunneling layer.

With respect to claim 2, AAPA further teaches the gate electrode 40 extends on the at least two trap sections.

With respect to claim 3, AAPA fails to teach the tunneling film is made of silicon oxide.

However, the use of silicon oxide as tunneling material is well-known.

With respect to claims 9, 20, and 48, AAPA fails to teach the carrier trap section or layer is made of silicon.

Mort et al. teach using amorphous silicon material to improve carrier trap. See col. 5, lines 55-65.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use silicon material to improved carrier trap ability in the device of AAPA.

Allowable Subject Matter

4. Claims 17, 18, and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP